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A TDK Group Company

SSI 75T201
Integrated DTMF Receiver

October 1991

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DESCRIPTION

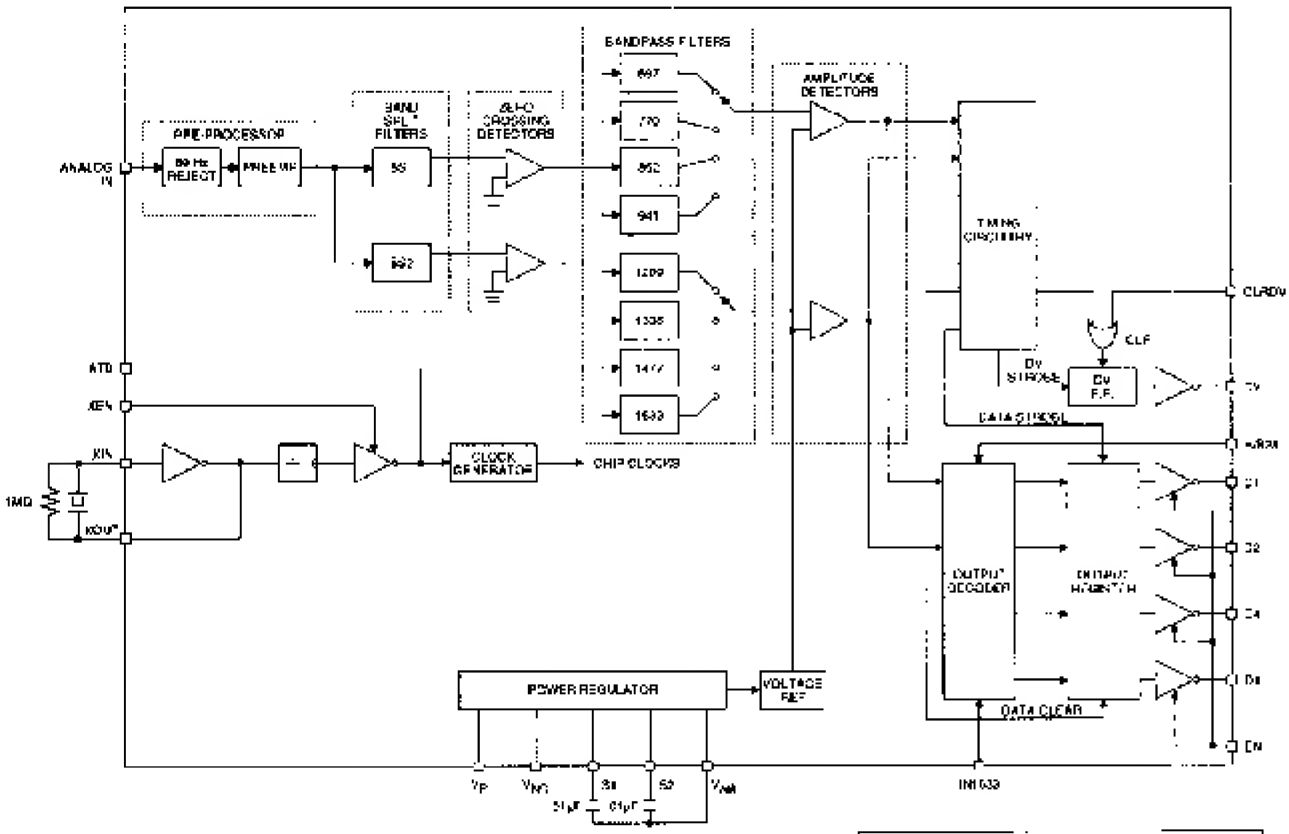
The SSI 75T201 is a complete Dual-Tone Multifrequency (DTMF) receiver detecting a selectable group of 12 or 16 standard digits. No front-end prefiltering is needed. The only external components required are an inexpensive 3.58 MHz television "colorburst" crystal (for frequency reference) and two low-tolerance bypass capacitors. Extremely high system density is made possible by using the clock output of a crystal connected SSI 75T201 receiver to drive the time bases of additional receivers. The SSI 75T201 is a monolithic integrated circuit fabricated with low-power, complementary symmetry MOS (CMOS) processing. It requires only a single low tolerance voltage supply and is packaged in a standard 22-pin DIP.

(Continued)

FEATURES

- Central office quality
- NO front-end band-splitting filters required
- Single, low-tolerance, 12-volt supply
- Detects either 12 or 16 standard DTMF digits
- Uses inexpensive 3.579545 MHz crystal for reference
- Excellent speech immunity
- Output in either 4-bit hexadecimal code or binary coded 2-of-8
- 22-pin DIP package for high system density
- Synchronous or handshake interface
- Three-state outputs

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 75T201 employs state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is preprocessed by 60 Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

CRYSTAL OSCILLATOR

The SSI 75T201 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T201's may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Twenty-five devices may run off a single crystal-connected SSI 75T201 as shown in Figure 2.

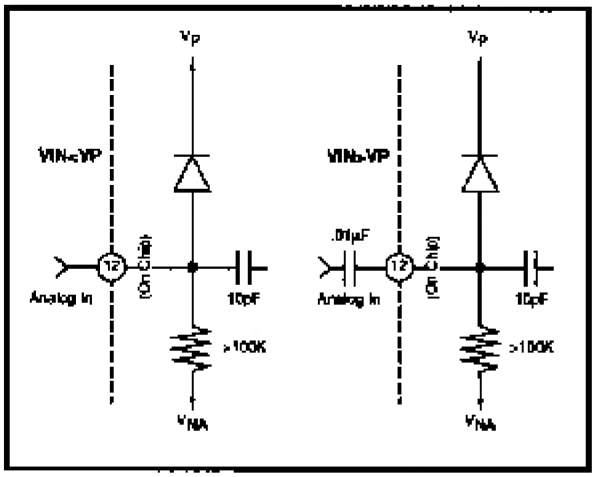


FIGURE 1: Input Coupling

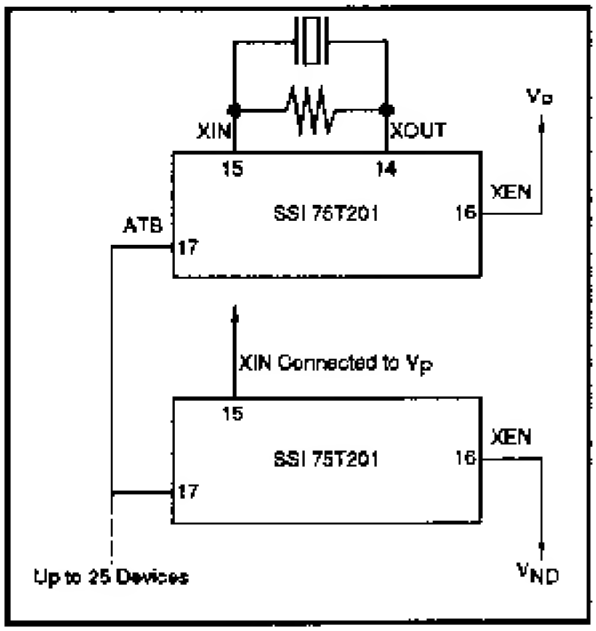


FIGURE 2: Crystal Connections

H/B28

This pin selects the format of the digital output code. When H/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The table below describes the two output codes.

Hexadecimal					Binary Coded 2-of-8				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	2	0	0	0	1
3	0	0	1	1	3	0	0	1	0
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	1	0	0	0
8	1	0	0	0	8	1	0	0	1
9	1	0	0	1	9	1	0	1	0
0	1	0	1	0	0	1	1	0	1
*	1	0	1	1	*	1	1	0	0
#	1	1	0	0	#	1	1	1	0
A	1	1	0	1	A	0	0	1	1
B	1	1	1	0	B	0	1	1	1
C	1	1	1	1	C	1	0	1	1
D	0	0	0	0	D	1	1	1	1

TABLE 1: Output Codes

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633 Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, and D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the H/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever comes first.

INTERNAL BYPASS PINS, S1, S2

In order for the SSI 75T201 DTMF Receiver to function properly, these pins must be bypassed to V_{NA} with 0.01 µF ±20% capacitors.

POWER SUPPLY PINS, V_P, V_{NA}, V_{ND}

The analog (V_{NA}) and digital (V_{ND}) supplies are brought out separately to enhance analog noise immunity on the chip. V_{NA} and V_{ND} should be connected externally as shown in Figure 3.

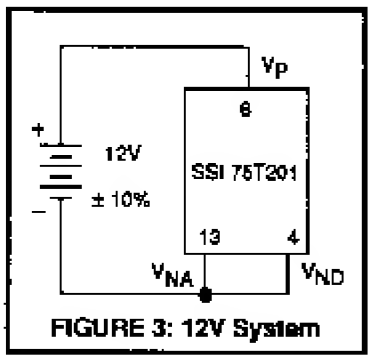


FIGURE 3: 12V System

N/C PINS

These pins have no internal connection and may be left floating.

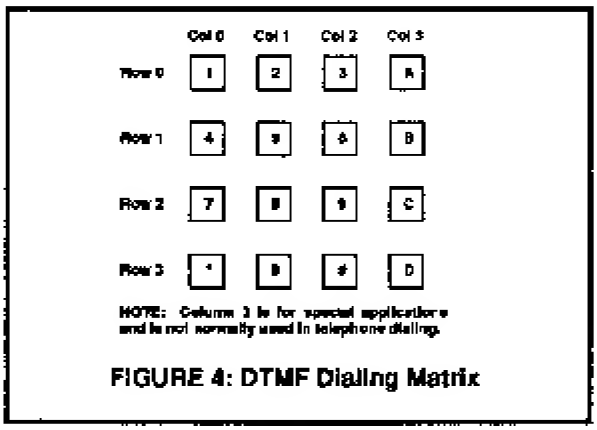


FIGURE 4: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_o	High Group f_o
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may damage the device. All SSI 75T201 unused inputs must be connected to V_P or V_{ND}, as appropriate.

PARAMETER	RATING	UNIT
DC Supply Voltage - V_P	Referenced to V_{NA}, V_{ND}	+16V
Operating Temperature		-40 to +85°C Ambient
Storage Temperature		-65 to +150°C
Power Dissipation (25°C)		1W
Input Voltage	All inputs except ANALOG IN	(V_P+ 0.5V) to (V_{ND} -0.5V)
ANALOG IN Voltage		(V_P + 0.5V) to (V_P - 22V)
DC Current into any Input		±1.0 mA
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

(-40°C ≤ Ta ≤ +85°C, V_P - V_{ND} = V_P - V_{NA} = 12V ± 10%)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		± (1.5+2 Hz)	±2.3	±3.0	% of f_D
Amplitude for Detection	each tone	-24		+6	dBm ref. to 600Ω
Twist Tolerance	Twist = High Tone / Low Tone	-8		+4	dB
60 Hz Tolerance				2	Vrms
Dial Tone Tolerance	"precise" dial tone			0	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 750 µA load	V_{ND}		V_{ND}+0.5	V
(except XOUT)	"1" level, 750 µA load	V_P-0.5		V_P	V
Digital Inputs	"0" level	V_{ND}		**	V
(except H/B28, XEN)	"1" level	***		V_P	V
Digital Inputs	"0" level	V_{ND}		V_{ND}+1	V
H/B28, XEN	"1" level	V_P-1		V_P	V
Power Supply Noise	wide band			25	mVp-p
Supply Current	Ta = 25°C V_P - V_{NA} = V_P - V_{ND} = 12V±10%		29	50	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P$ - 22	100 kΩ‖5 pF			

* dB referenced to lowest amplitude tone
** V_{ND} + 0.3(V_P - V_{ND})
*** V_P - 0.3(V_P - V_{ND})

TIMING CHARACTERISTICS

(-40°C ≤ Ta ≤ +85°C, V_P - V_{ND} = V_P - V_{NA} = 12V ± 10%)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
tv	Tone Detection Time		20	25	40	ms
tsh	Data Overlap of DV Rising Edge	CLRDV = V_{ND}, EN = V_P	7			µs
tp	Pause Detection Time		25	32	40	ms
tdv	Time between end of Tone and Fall of DV		40	45	50	ms

TIMING CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{shl}	Data overlap of DV Falling Edge		4	4.56	4.8	ms
t_{phl}	Prop. Delay: Rise of CLRDV to fall of DV	Cl = 300 pF Measured at 50% points			1	µs
	Output Enable Time	Cl = 300 pF, Rl = 10K Measured from 50% point of Rising Edge of EN to the 50% point of the data output with Rl to opposite rail.			1	µs
	Output Disable Time	Cl = 300 pF, Rl = 1K, ΔV = 1V Measured from 50% point of Falling Edge of EN to time at which output has changed 1V with Rl to opposite rail.			1	µs
	Output 10-90% Transition Time	Cl = 300 pF			1	µs

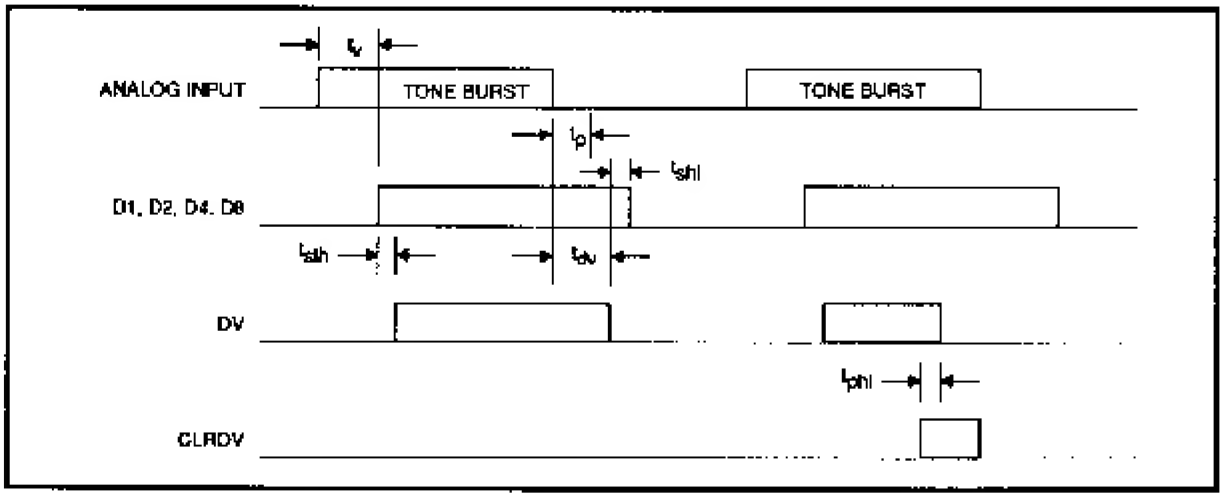


FIGURE 5: Timing Diagram

APPLICATION INFORMATION

TELEPHONE LINE INTERFACE

In applications that use the SSI 75T201 to decode DTMF signals from a phone line, a DAA (Direct Access Arrangement) must be implemented. Equipment intended for connection to the public telephone network must comply with and be registered in accordance with FCC Part 68. For PBX applications refer to EIA Standard RS-464.

Some of the basic guidelines are:

1) Maximum voltage and current ratings of the SSI 75T201 must not be exceeded; this calls for protection from ringing voltage, if applicable, which ranges from 80 to 120 volts RMS over a 20 to 80Hz frequency range.

2) The interface equipment must not breakdown with high-voltage transient tests (including a 2500 volt peak surge) as defined in the applicable document.

3) Phone line termination must be less than 200Ω DC and approximately 600Ω AC (200-3200 Hz).

4) Termination must be capable of sustaining phone line loop current (off-hook condition) which is typically 18 to 120 mA DC.

5) The phone line termination must be electrically balanced with respect to ground.

6) Public phone line termination equipment must be registered in accordance to FCC Part 68 or connected through registered protection circuitry. Registration typically takes about six months.

Figure 6 shows a simplified phone line interface using a 600Ω 1:1 line transformer. Transformers specially designed for phone line coupling are available from many transformer manufacturers.

Figure 7 shows a more featured version of Figure 6. These added options include:

1) A 150-volt surge protector to eliminate high voltage spikes.

2) A Texas Instruments TCM1520A ring detector, optically isolated from the supervisory circuitry.

3) Back-to-back Zener diodes to protect the DTMF (and optional multiplexer Op-Amp) from ringer voltage.

4) Audio multiplexer which allows voice or other audio to be placed on the line (a recorded message, for example) and not interfere with incoming DTMF tone detection.

An integrated voice circuit may also be implemented for line coupling, such as the Texas Instruments TCM1705A, however, this approach is typically more expensive than using a transformer as shown above.

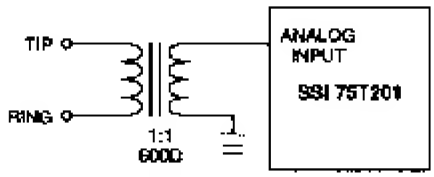


FIGURE 6: Simplified Interface

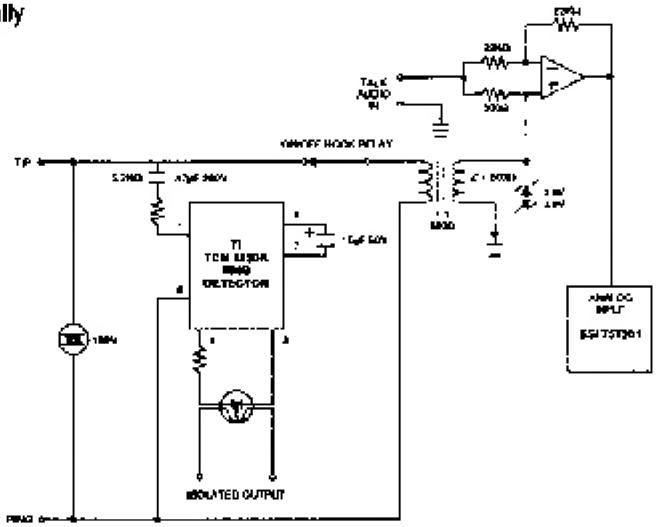
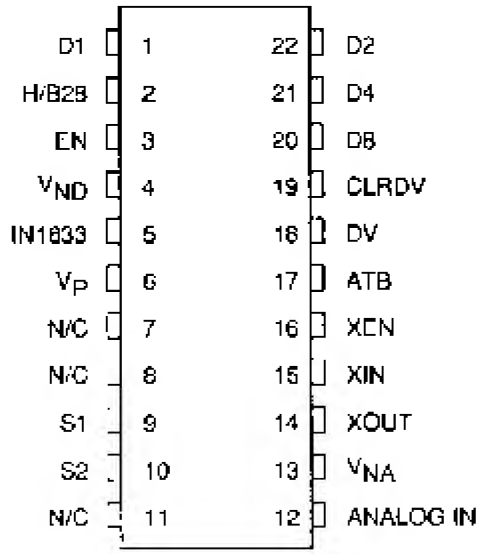


FIGURE 7: Full Featured Interface

SSI 75T201
Integrated
DTMF Receiver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



22-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T201 22-Pin Plastic DIP	75T20* - IP	75T201 - IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000 FAX: (714) 573-6914